REMARKS

The amendments suggested by the examiner have been made, as well as a few additional amendments to the claims. Claim 2 has been canceled and the required adjustments to the dependency of other claims have been made. Thus, it is believed that the rejections under 35 USC § 112 have been overcome.

Claims 1-10 and 13 have been rejected as being unpatentable over Asai et al (WO 98/27798; English translation, U.S. Patent 6,835,895) hereinafter Asai et al, in view of Chen et al, U.S. Patent 5,156,710, hereinafter Chen et al. (The U.S. patent to Asai et al has been relied on for all discussion of Asai et al.) This rejection is not thought to be well taken, especially in view of the amendments to the claims.

First, claim 1, as amended, the only independent claim in the application, specifically claims selectively roughening some, but not the entire signal plane, including the lands, to a roughness greater than the remainder of the surface thereof and specifically requires the use of a sticker sheet in the lamination process. It is submitted that neither Asai et al nor Chen et al teach or suggest these limitations and, thus, claim 1 is clearly allowable over any reasonable combination of these two references.

First it should be noted that claim 1, as amended, requires the roughening of some, but less than all, including the lands, of the surface of the signal plane. The reason for this and the solution is clearly brought out on page 2, lines 10-19, of the application as follows:

> It has been found that roughening of the conductors on the printed wiring board structure is critical only in certain regions and not required for the entire length of each of the circuit traces or signal lines. In fact, the mechanical and chemical exposures are greatest where a signal or power plane intersect a plated through hole. Therefore, the need is greater for good copper to laminate adhesion at this intersection than in the open, non-drilled areas of the board. Thus, according to the present invention, a printed wiring board is formed from two or more layers, one of which has circuit lines formed thereon, and wherein the surfaces of the circuit lines or traces are

selectively roughened only in those areas that require very good copper to laminate adhesion, whereas the remainder of the surface of the circuit lines or traces are maintained in essentially a smooth condition.

While Asai et al indicate that less than the entire surface *may be* roughened, this is not a requirement, and certainly there is no *requirement* that the lands be roughened. Moreover, the examiner states that Chen et al teach a "sticker sheet". "Sticker sheet" clearly implies that the sticker sheet is separate from the other parts, and Chen et al teach an integral film formed on the substrate, both at the location cited by the examiner as well as the description of the preferred embodiment. Thus, claim 1 is clearly allowable over any reasonable combination of Asai et al and Chen et al.

The subject matter of claim 2, but corrected as suggested by the examiner, has been included in amended claim 1 and, thus, claim 2 has been canceled. Claims 3-10, 12-13 and 15 are dependent directly or indirectly on claim 1 and, for the same reasons, are believed to be allowable.

Moreover, with respect to claims 3-5, these claims require a certain degree of roughening. The examiner states that Figure 4 of Asai et al teaches this or, alternatively, selecting the amount of roughening would have been obvious to a person skilled in the art. It is not believed that either of these positions is tenable. First, Figure 4 does not suggest any degree of roughening and, second, there is no reason that a person skilled in the art would select these values out of the myriad of possibilities. And, the examiner has given no reason for such selection other than it would work. It is submitted that this is not an acceptable reason. Thus, for this additional reason, claims 3-5 are believed to be allowable.

With respect to claim 8, the examiner takes the position that it would be obvious to provide first and second portions of the voltage plane with different roughnesses, but gives no

supporting reason therefor. It is submitted, however, that it is the inventors who have discovered that the entire plane does not need the rougher surface, and there is nothing obvious about it. Claim 9 recites a specific value for the roughness and, as pointed out above, there is nothing in Figure 4 which indicates any values, and there is noting obvious about the values.

The examiner has rejected claims 12 and 15 under 35 U.S.C. §103(a) as being unpatentable over Asai et al and Chen et al and further in view of Tippner et al, U.S. Patent 6,175,085, bereinafter Tippner et al. This rejection is not thought to be well taken. First, these claims are dependent on claim 1 and, for the same reasons, are believed to be allowable. In addition, in Tippner et al, the covering is not the same as in the applicants' process and, thus, is not apropos.

For all the above reasons, it is believed that each of the claims now in the application is distinguishable one from the other and over the prior art. Therefore, reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

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